UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,078	08/22/2003	Andrew H. Barr	200206932-1	9606

22879 7590 03/02/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,078	BARR ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 40 are presented for the examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 13 January 2005 was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claims 6, 8 – 9, 17, 26 – 27, and 36 are objected to because of the following informalities:

4. Claims 6, 8 – 9, and 26 – 27, recites the limitation "I/O device" on line 2, of pages 18 and 19. The abbreviation of term "I/O device" is required or defined at least once in claim.

5. Claims 17, and 36, recites the limitation "DIP switch" on line 1, of pages 20 and 23. The abbreviation of term "DIP switch" is required or defined at least once in claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1 – 23 are rejected under 35 U.S.C. 101 because the language of the claims 1, and 22 "automatically selecting a first clock frequency for the first electronic device and a second clock frequency for the second electronic device, based at least on

information about the application program" raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible results to form the basis of statutory subject matter under 35 U.S.C. 101.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1 – 40, provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 - 31 of copending Application No. 10/646099, and claims 1 – 54 of copending Application No. 10/646079. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

8. The independent claim 1 of current application, for method of determining a clock frequency for first and second electronic device including automatically selecting a first and second clock frequency for first and second device and supplying to first and second device respectively is almost identical to claim 1 of pending application 10/646099 and claim 28 of pending application 10/646079.

9. The independent claim 22 of current application, an article manufacturer including a computer –readable medium for storing instructions capable of determining a clock frequency for first and second electronic device including automatically selecting a first and second clock frequency for first and second device and supplying to first and second device respectively is almost identical to claim 17 of pending application 10/646099 and claim 42 of pending application 10/646079.

10. The independent claim 23 of current application, a frequency manager for determining a clock frequency for first and second electronic device including frequency calculator automatically selecting a first and second clock frequency for first and second device and supplying to first and second device respectively is almost identical to claim 18 of pending application 10/646099 and claim 43 of pending application 10/646079.

11. The dependent claims 2 – 21, and 24 - 40 of the current application are almost similar to the claims 2 – 16, 19 – 31 of pending application 10/646099 and 17 – 27, 29 – 41, and 44 – 54, of pending application 10/646079.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 23 – 26, 28, 32 – 37, 39, and 40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Iwazaki, US Patent 6,073,244.

13. As to claim 23, Iwazaki discloses a frequency manager [4, clock control circuit] for determining a clock frequency for a first electronic device [2, CPU] and a clock frequency for a second electronic device [31 peripheral processing unit], the first and second electronic devices being installed in a system [information processing system] with zero or more other electronic devices, the first electronic device [2] being connected to a first bus [system bus] and the second electronic device [31, 32] being connected to a second bus [peripheral bus], the system being capable of executing an application program [inherent to the information processing, col. 5, lines 61 – 62, fig. 5], comprising:

a. a frequency calculator [41A, 41, clock selection and control unit] automatically selecting a first clock frequency for the first electronic device [2, CPU] and a second clock frequency for the second electronic device [31, 32, peripheral unit], based at least on information about [the load state] the application program [on CPU, and peripheral device]; and

b. an interface [45A, 45] connected to the frequency calculator [4], to a first clock signal generator [1A] and to a second clock frequency generator [1], the interface

sending commands [instructions] [col. 9, lines 64 – 67, col. 10, lines 1 – 9]: to the first clock signal generator [1A] to generate clock signals at the first clock frequency and to the second clock frequency generator to generate clock signals at the second clock frequency][col. 4, lines 4 – 23, col. 6, lines 44 – 67, col. 7, lines 1 – 23, col. 9, lines 1 – 38, and 64 – 67, col. 10, lines 1 – 9, fig. 5].

14. As to claim 24, Iwazaki discloses the frequency calculator [41A, 41, clock selection and control unit] further bases the automatically selecting a first and second clock frequency on information about [load state] the first and second electronic devices and the zero or more other electronic devices installed in the system [col. 9, lines 1 – 38, and 64 – 67, col. 10, lines 1 – 9, fig. 5 – 7].

15. As to claim 26, Iwazaki discloses apparatus and method for information processing including memory and input/output device [fig. 9].

16. As to claim 25, Iwazaki discloses that the information about relative loads [load state] the application program places on the first [2] and second devices [31, 32] [col. 9, lines 64 – 67, col. 10, lines 1 – 9].

17. As to claim 30, Iwazaki discloses the frequency manager [4], the information about [the load state] the first [2] and second electronic devices [31, 32] and the zero or more other electronic devices comprises a number of the other electronic devices [peripheral processing unit inherently comprises number of other electronic devices] installed in the system [fig. 5 – 7].

18. As to claim 32, Iwazaki discloses the frequency manager [4], the frequency calculator [41A, 41] further bases the automatically selecting a first and second clock frequency on a power consumption budget for the system [col. 3, lines 7 – 12].

19. As to claim 33, Iwazaki discloses the frequency manager [4] including an information input [bus access rate] automatically ascertaining [34 bus access monitoring unit] at least some of the information about [the load state] the first [2] and second electronic devices [31, 32] [col. 6, lines 44 – 65, col.9, lines 23 – 38].

20. As to claim 34, Iwazaki discloses the frequency manager [4] including a bus access monitoring unit [44] for the information input [bus access rate] queries at least one of the first and second electronic devices to ascertain the at least some of the information about the first and second electronic devices [col. 6, lines 44 – 65, col.9, lines 23 – 38].

21. As to claim 35, Iwazaki discloses an information processing apparatus including a memory [103] for storing information about the first and second electronic devices [fig. 9].

22. As to claim 36, Iwazaki discloses an information processing apparatus including a memory [103 fig. 9], which inherently comprises a DIP switches.

23. As to claim 37, Iwazaki discloses an information processing apparatus including a peripheral processing unit [31, 32] which inherently comprises a user interfaces [keyboard, mouse] to ascertain some information about first [2] and second electronic [31, 32] devices [fig. 5, 9].

24. As to claims 39, and 40, Iwazaki teaches information processing apparatus including peripheral processing unit [31, 32], which inherently teaches removably installed device in an expansion slot.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. Claims 27 – 29, 31, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki, US Patent 6,073,244 as applied to claim 23, and further in view of Dai, US Patent 6,714,890 B2.

26. As to claims 27 – 29, Iwazaki discloses a frequency manager [4, clock control circuit] for determining a clock frequency for a first electronic device [2, CPU] and a clock frequency for a second electronic device [31 peripheral processing unit], the first and second electronic devices being installed in a system [information processing system] with zero or more other electronic devices, the first electronic device [2] being

connected to a first bus [system bus] and the second electronic device [31, 32] being connected to a second bus [peripheral bus], the system being capable of executing an application program [inherent to the information processing, col. 5, lines 61 – 62, fig. 5], comprising: a frequency calculator [41A, 41, clock selection and control unit] automatically selecting a first clock frequency for the first electronic device [2, CPU] and a second clock frequency for the second electronic device [31, 32, peripheral unit], based at least on information about [the load state] the application program [on CPU, and peripheral device]; and an interface [45A, 45] connected to the frequency calculator [4], to a first clock signal generator [1A] and to a second clock frequency generator [1], the interface sending commands [instructions] [col. 9, lines 64 – 67, col. 10, lines 1 – 9]: to the first clock signal generator [1A] to generate clock signals at the first clock frequency and to the second clock frequency generator to generate clock signals at the second clock frequency][col. 4, lines 4 – 23, col. 6, lines 44 – 67, col. 7, lines 1 – 23, col. 9, lines 1 – 38, and 64 – 67, col. 10, lines 1 – 9, fig. 5].

However, Iwazaki does not teach automatically selecting a first and second clock frequency based on an application program category [enhanced speed state].

Dai discloses a method and apparatus and machine readable medium to enhance microprocessor performance by determining an enhanced speed state from instruction mix to dynamically adapt different microprocessor-operated devices having different operating conditions [col. 8, lines 27 – 60] [changing the operation of processor by changing the operating frequency based on speed state][col. 5, lines 9 – 29,col. 6, lines 55 – 67, col. 8, lines 41 – 60, fig. 2B, 4 – 5].

It would have been obvious to one of ordinary skill in art, having the teachings of Iwazaki and Dai before him at the time of invention was made, to modify the clock control and selection as disclosed by Iwazaki to include enhanced speed state controller to change the operating frequency based on an application program category [speed state] as taught by Dai, in order to obtain clock control apparatus and method to enhance the performance of processor with compromise an enhanced speed state and a lower power dissipation state [col. 5, lines 55 – 65] and by monitoring an output on-die reduces the latency and facilitate preventing the temperature of microprocessor from rising to a damage temperature [col. 5, lines 1 – 8, col. 7, lines 31 – 64].

27. As to claims 28 – 29, Dai discloses speed state controller including determining different speed state with instruction mix [application program category] therefore he teaches more memory intensive than input/Output intyensive, and more input/Output intensive than memory too.

28. As to claims 31, and 38, Iwazaki discloses a frequency manager [4, clock control circuit] for determining a clock frequency for a first electronic device [2, CPU] and a clock frequency for a second electronic device [31 peripheral processing unit], the first and second electronic devices being installed in a system [information processing system] with zero or more other electronic devices, the first electronic device [2] being connected to a first bus [system bus] and the second electronic device [31, 32] being connected to a second bus [peripheral bus], the system being capable of executing an application program [inherent to the information processing, col. 5, lines 61 – 62, fig. 5], comprising: a frequency calculator [41A, 41, clock selection and control unit]

automatically selecting a first clock frequency for the first electronic device [2, CPU] and a second clock frequency for the second electronic device [31, 32, peripheral unit], based at least on information about [the load state] the application program [on CPU, and peripheral device]; and an interface [45A, 45] connected to the frequency calculator [4], to a first clock signal generator [1A] and to a second clock frequency generator [1], the interface sending commands [instructions] [col. 9, lines 64 – 67, col. 10, lines 1 – 9]: to the first clock signal generator [1A] to generate clock signals at the first clock frequency and to the second clock frequency generator to generate clock signals at the second clock frequency][col. 4, lines 4 – 23, col. 6, lines 44 – 67, col. 7, lines 1 – 23, col. 9, lines 1 – 38, and 64 – 67, col. 10, lines 1 – 9, fig. 5].

However, Iwazaki does not teach automatically selecting a first and second clock frequency based on a thermal budget for the system.

Dai discloses a method and apparatus to manage a temperature of the microprocessor by determining the temperature of processor reached a trigger temperature [thermal budget] and changing the operation of processor to lower power dissipation state by changing the operating frequency [col. 3, lines 9 – 1528 – 35, col. 4, lines 26 – 53].

It would have been obvious to one of ordinary skill in art, having the teachings of Iwazaki and Dai before him at the time of invention was made, to modify the clock control and selection as disclosed by Iwazaki to include changing the operating frequency based on the a temperature trigger reached or heat dissipation [thermal budget] as taught by Dai, in order to obtain clock control apparatus and method to

enhance the performance [abstract] of processor and by monitoring an output on-die reduces the latency and facilitate preventing the temperature of microprocessor from rising to a damage temperature [col. 5, lines 1 – 8, col. 7, lines 31 – 64].

29. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

30. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
January 30, 2006

JOHN R. COTTINGHAM
PRIMARY EXAMINER